

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

- AI
1. (currently amended): A graphics accelerator, comprising:
 - a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined graphics accelerator architecture; and
 - a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a local-buffer memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
 2. (original): The accelerator of Claim 1, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

3. (currently amended): A graphics accelerator, comprising:

a plurality of specialized processing subunits,
interconnected through a serial message-passing interface to provide
a reconfigurably pipelined graphics accelerator architecture;
at least one of said specialized processing subunits comprising
multiple subprocessors connected to operate in parallel on
separate tasks; and
a high bandwidth memory interface independent of said serial message-
passing interface which interfaces to ~~local buffer~~ a memory of
said graphics accelerator, said memory capable of storing
displayable pixel information;

wherein said serial interface also permits downloading of image data to
ones of said subunits.

4. (currently amended): The accelerator of Claim [[1]]3, wherein ones of
said subunits are configured so that said memory interface accesses
multiple tiles of pixels simultaneously.

5. (new): The accelerator of Claim 3, wherein ones of said subunits are
configured so that said memory interface accesses multiple byte-sized
tiles of pixels simultaneously.

6. (new): The accelerator of Claim 3, wherein said subunits include a
current parameter unit, a vertex shading unit, a vertex machine unit, a
cull unit, and a geometry unit.

7. (new): The accelerator of Claim 1, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
8. (new): The accelerator of Claim 1, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
9. (new): A graphics rendering system comprising:
a host processor;
a system memory; and
a graphics accelerator comprising:
a plurality of specialized processing subunits, interconnected through a message-passing interface to provide a generally pipelined graphics accelerator architecture; and
a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
10. (new): The system of Claim 9, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.
11. (new): The system of Claim 9, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.

12. (new): The system of Claim 9, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.

13. (new): A graphics rendering system comprising:

A/ a host processor;

a system memory; and

a graphics accelerator comprising:

a plurality of specialized processing subunits,

interconnected through a serial message-passing interface to provide

a reconfigurably pipelined graphics accelerator architecture;

at least one of said specialized processing subunits comprising

multiple subprocessors connected to operate in parallel on separate tasks; and

a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information;

wherein said serial interface also permits downloading of image data to ones of said subunits.

14. (new): The system of Claim 13, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

15. (new): The system of Claim 13, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
16. (new): The system of Claim 13, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
17. (new): A computing system for graphics rendering, the system comprising:
a host processor;
a system memory; and
a computer graphics pipeline coupled to said host processor;
the computer graphics pipeline comprising:
a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined graphics accelerator architecture; and
a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
18. (new): The system of Claim 17, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

19. (new): The system of Claim 17, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
20. (new): The system of Claim 17, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
21. (new): A computing system for graphics rendering, the system comprising:
- a host processor;
 - a system memory; and
 - a computer graphics pipeline coupled to said host processor;
- the computer graphics pipeline comprising:
- a plurality of specialized processing subunits,
 - interconnected through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator architecture;
 - at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and
 - a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information;
- wherein said serial interface also permits downloading of image data to ones of said subunits.

27. (new): The method of Claim 25, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.

28. (new): The method of Claim 25, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.

29. (new): A method of designing graphics accelerators, comprising the steps of:

interconnecting a plurality of specialized processing subunits through a serial message-passing interface to provide a reconfigurably pipelined graphics accelerator;

at least one of said specialized processing subunits comprising multiple subprocessors connected to operate in parallel on separate tasks; and

providing a interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator through a memory interface, said memory capable of storing displayable pixel information;

wherein said serial interface also permits downloading of image data to ones of said subunits.

30. (new): The method of Claim 29, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

22. (new): The system of Claim 21, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

23. (new): The system of Claim 21, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.

24. (new): The system of Claim 21, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.

25. (new): A method of designing graphics accelerators, comprising the steps of:

interconnecting a plurality of specialized processing subunits through a serial message-passing interface to provide a generally pipelined graphics accelerator; and

providing a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator through a memory interface, said memory capable of storing displayable pixel information.

26. (new): The method of Claim 25, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.

31. (new): The method of Claim 29, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.
32. (new): The method of Claim 29, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
33. (new): A graphics rendering method, comprising the steps of:
receiving graphics primitives; and
sending said graphics primitives through a graphics accelerator comprising:
a plurality of specialized processing subunits, interconnected through a serial message-passing interface to provide a generally pipelined architecture; and
a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information.
34. (new): The method of Claim 33, wherein ones of said subunits are configured so that said memory interface accesses multiple tiles of pixels simultaneously.
35. (new): The method of Claim 33, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.

36. (new): The method of Claim 33, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.

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37. (new): A graphics rendering method, comprising the steps of:
receiving graphics primitives; and
sending said graphics primitives through a graphics accelerator comprising:
a plurality of specialized processing subunits,
interconnected through a serial message-passing interface to provide
a reconfigurably pipelined graphics accelerator architecture;
at least one of said specialized processing subunits comprising
multiple subprocessors connected to operate in parallel on
separate tasks; and
a high bandwidth memory interface independent of said serial
message-passing interface which interfaces directly to a
memory of said graphics accelerator, said memory capable of
storing displayable pixel information;
wherein said serial interface also permits downloading of image data
to ones of said subunits.

38. (new): The method of Claim 37, wherein ones of said subunits are
configured so that said memory interface accesses multiple tiles of
pixels simultaneously.

39. (new): The method of Claim 37, wherein ones of said subunits are configured so that said memory interface accesses multiple byte-sized tiles of pixels simultaneously.

40. (new): The method of Claim 37, wherein said subunits include a current parameter unit, a vertex shading unit, a vertex machine unit, a cull unit, and a geometry unit.
